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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/485,443	05/01/2000	WEI CHEN	Q57774	1926

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EXAMINER

KING, JUSTIN

ART UNIT PAPER NUMBER

2181

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/485,443

Applicant(s)

CHEN ET AL.

Examiner

Justin I. King

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☒ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (U.S. Patent No. 6,311,245).

Klein discloses a bus system accommodating both high speed and low speed devices. Klein discloses that a computer architect is able to isolate certain high volume or time critical data exchanges between particular devices from lower volume or less critical data exchange (column 2, lines 4-6). The I/O speed has been an industrial bottleneck for the computer performance. In order to accommodate CPU, cache and RAM's high speed, it has been a common practice for computer architects to adapt a separate high-speed local bus; Klein discloses that it is well known to one in the computer art to manage the system's overall performance by categorizing each device's transmission speed. Klein further discloses that it is a

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common practice to have two PCI buses to support low-speed devices and high-speed devices separately (figure 1). Although Klein does not disclose a serial bus, Klein discloses that it is known to optimize the overall system performance by arranging devices based on their transmission speed.

“Official Notices” are taken on the following:

1. Due to the serial bus’ design and physical restriction, it is inherent that a child node’s performance can be affected or undercut by the transmission speed of its parent node and nodes in the hopping path. The common industrial local bus design teaches that it is ideal to place the higher-speed devices closer to the CPU because the CPU is where the instructions are initiated and it reduces the transmission latency. Analogously, it would be obvious to one in the computer art to connect a higher-speed devices closer to the serial bus connector because the serial bus connector is where the serial bus’ instructions are initiated, and this arrangement will also minimize the parent nodes’ effect on the child nodes’ performance due to various transmission speed. In addition, the number of ports of each device also has an inherent effect on overall system performance. The number of ports correlates to the maximum number of child nodes, such that more child nodes can be connected closer to the serial bus connector and it avoids the child nodes’ extra hops if they were connected further down in the serial bus.

2. It is known to one in the computer art that any given node in a serial bus, except the beginning node and the ending node, must have at least 2 ports for connecting to its parent node and child node. Such that, It is obvious to one in the computer art that a serial bus with N number of nodes will need to have at least $2N$ ports minus one port from each of the beginning node and the ending node, which concludes the total number of $2N-2$ ports, which equals to $2(N-1)$ ports.

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Although both of the devices' speed and port number have inherent impact on system performance, the devices' speed provides a more concrete foundation for directly comparison on the each device's speed capacity. The port number provides the potential possible connections, but until the completion of the serial bus circuit, it is uncertain on how many ports will be connected; in addition, every child node's performance will be affected by this device's speed capacity.

Hence, it would be obvious to one having ordinary skill in the computer art at the time applicant made the invention to adapt the teachings of Klein and the common industrial practices into a serial bus connection because they teach one to minimize the potential impact from the variation of each device's transmission speed.

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Conclusion

4. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,559,967 to Opreescu et al.: Opreescu teaches the effect of a low transmission speed device in a serial bus, and teaches a method to overcome the potential impact by modifying the message.

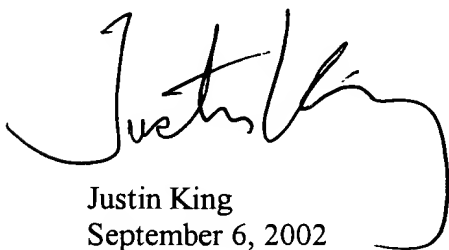
U.S. Patent No. 5,533,198 to Thorson, Gregory M.: Thorson teaches the relationship between the hopping and latency, and teaches a multiple dimensional topology to reduce the latency.

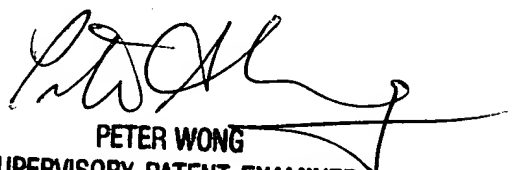
U.S. Patent No. 6,094,700 to Deschepper et al.: Deschepper teaches a method to synchronize a serial bus' transmission.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Peter Wong can be reached at (703) 305-3477.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.


Justin King
September 6, 2002


PETER WONG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100